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GENERAL ANALOG FUNCTIONS
A/D & D/A INTERFACES
ACTIVE FILTERS
PHASE-LOCKED LOOPS
MONOLITHIC & HYBRID
IMPLEMENTATIONS

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SUBJECT: NBS RECEIVER

The attached schematics show work completed to date on the NBS receiver circuit for use with very high accuracy clock products. The circuit is complete except for the design of two detector blocks for use in the AGC. Circuit operation will be described here in the event the the project is revived at some later date.

Refer to the schematics for component designations: Basically, the circuit is a phase-locked-loop receiver with coherent AGC and signal detection for best extraction of the signal from deep immersion in man-made noise (signal strength is not a problem except in the extreme East coast). A VCO capacitor (pin 5) is driven by current source Q_{29} in the positive-going direction; the voltage on this cap. is buffered thru Q_{28} to differential pair Q_{18}-Q_{17} which cause a Schmidt trigger composed of Q_{23}, Q_{22}, and Q_9 to trip when approximately 2/3 of the supply voltage is reached (Q_8 & Q_4 prevent saturation of driven stages - more on this later). Tripping of this trigger causes current source Q_{33}-Q_{32} to turn on slewing the cap. in the opposite direction until diff. pair Q_{21}-Q_{20} cause the trigger to reset and the cycle repeats, thus creating an oscillation action. Q_{31}, Q_{30}, Q_{36}, Q_{35}, Q_{34}, Q_{33}, & Q_{32} are tied together in a DC loop, such that only the value of the pot tied to pin 6 and the value of the VCO cap. determine the center

frequency of oscillations, virtually independent of power supply variations - all device parameters are designed out, assuming reasonable v_{BE} match and beta tracking. Devices Q_{27} & Q_{26} provide mid-point slicing of the capacitor ramp voltage, thus providing a signal 90° out of phase with the main VCO for use with the quadrature detector. Q_{25}, Q_{19}, Q_{16}, Q_{14}, Q_{15}, Q_{12} &Q_7 are bias elements for the diff. pairs and the Schmidt trigger. Q_8, Q_4, Q_3 & Q_2 together with load Q_1 buffer the trigger output to a level compatible with MOS logic (8V P-P). The form of Q_8 & Q_4 prevent saturation of Q_3 thus eliminating storage effects and provide a "glitchless", non-overlapping drive for the phase detector. Q_6 &Q_5 provide clamping of the output signal such that no circulating currents occur thru the package pins, thus avoiding magnetic radiation back to the input stage. Q_{37} thru Q_{50}, & Q_{53} thru Q_{56} provide a doubly balanced phase detector with no DC offset components to reduce signal detection capabilities (you must analyse it some time to believe it). This form of phase detector was used to allow convenient direct connection of tuning elements to ground for good shield, to reduce pin count, and to avoid additional capacitors and DC offset problems. Q_{13}, Q_{10}, Q_{11}, Q_{55} &Q_{56} couple the VCO to the phase detector in a DC compatible fashion while preventing additional saturation problems. Q_{45}, Q_{51} & Q_{52} comprise a DC loop, setting up the phase detector in a balanced condition. Signal applied to the base of Q_{44} unbalances the phase detector causing a DC signal to appear (filtered by lead-lag elements on pin 6) on the base of Q_{31} which is a part of the DC loop setting the VCO frequency - thus the VCO is always pulled away from its natural frequency when coming to lock. This technique provides maximum pull-in capability with minimum signal strength.

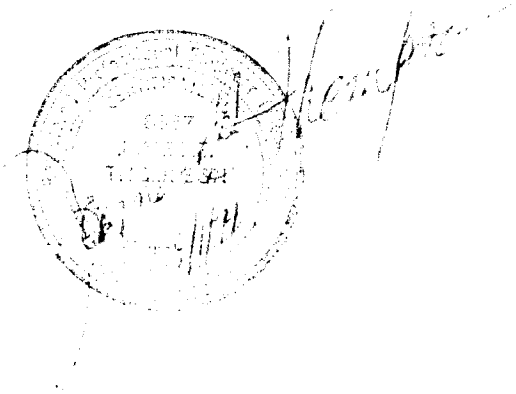
The second schematic details signal amplification stages, AGC, and signal detection. Q_{59} thru Q_{67} in conjunction with signals

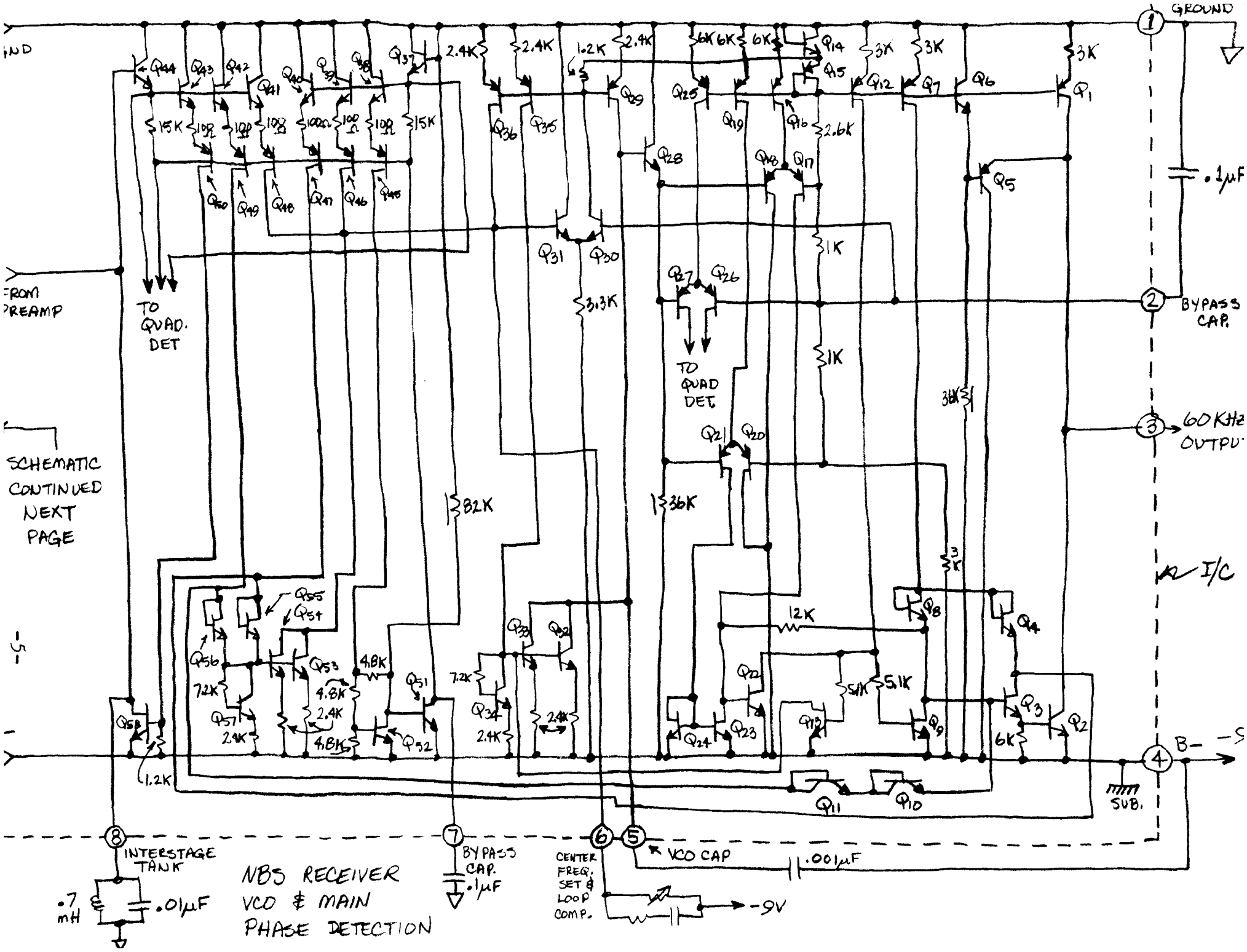
from Q_{26} & Q_{27} comprise a quadrature phase detector - thus the output is a direct function of signal amplitude and will therefore contain the modulation of interest - the one second cycles with pulse-width encoded BCD time information. This information will, however, be available only if the phase detector is operating in a region where it is able to handle the transmitted dynamic range of 12 dB. It is at this point that due consideration must be given to proper design of the AGC. These circuits had not been implemented at the time of project termination, but had been blocked out to the form shown in the schematic. Q_{68} thru Q_{71} are current steering AGC elements which can reduce the level of signal coming from Q_{72}-Q_{73}. Assume that element blocks "Max Signal Limiter" and "Minimum Signal Detector" are designed such that with no signal present, maximum gain occurs. Full signal will be applied to the main phase detector and phase lock will occur - overly large signals will be limited by Q_{50} &Q_{58} (see first schematic). When phase-lock occurs the quadrature detector will begin to detect modulation. If the minimum value of the modulation swing does not reach down to the level of the "Minimum Value Detector" the gain will be reduced (& vice versa) until it just does (imagine the "Minimum Value Detector" implemented as a negative-going peak-detector). Once this level is set (& held), the 12 dB excursions of the signal will rise high enough to trip the "Max Signal Limiter" which will reduce the gain to hold this upper level. Thus modulation can be held nicely between two prescribed limits, and with the overall AGC effect, the VCO will be held firmly in lock during modulation. Q_{78}, Q_{77}, Q_{73}, & Q_{72} form a preamplifier with 94 dB of gain. Q_{75}, Q_{76} & Q_{74} provide bias for this stage, such that the input loop can be direct coupled in.

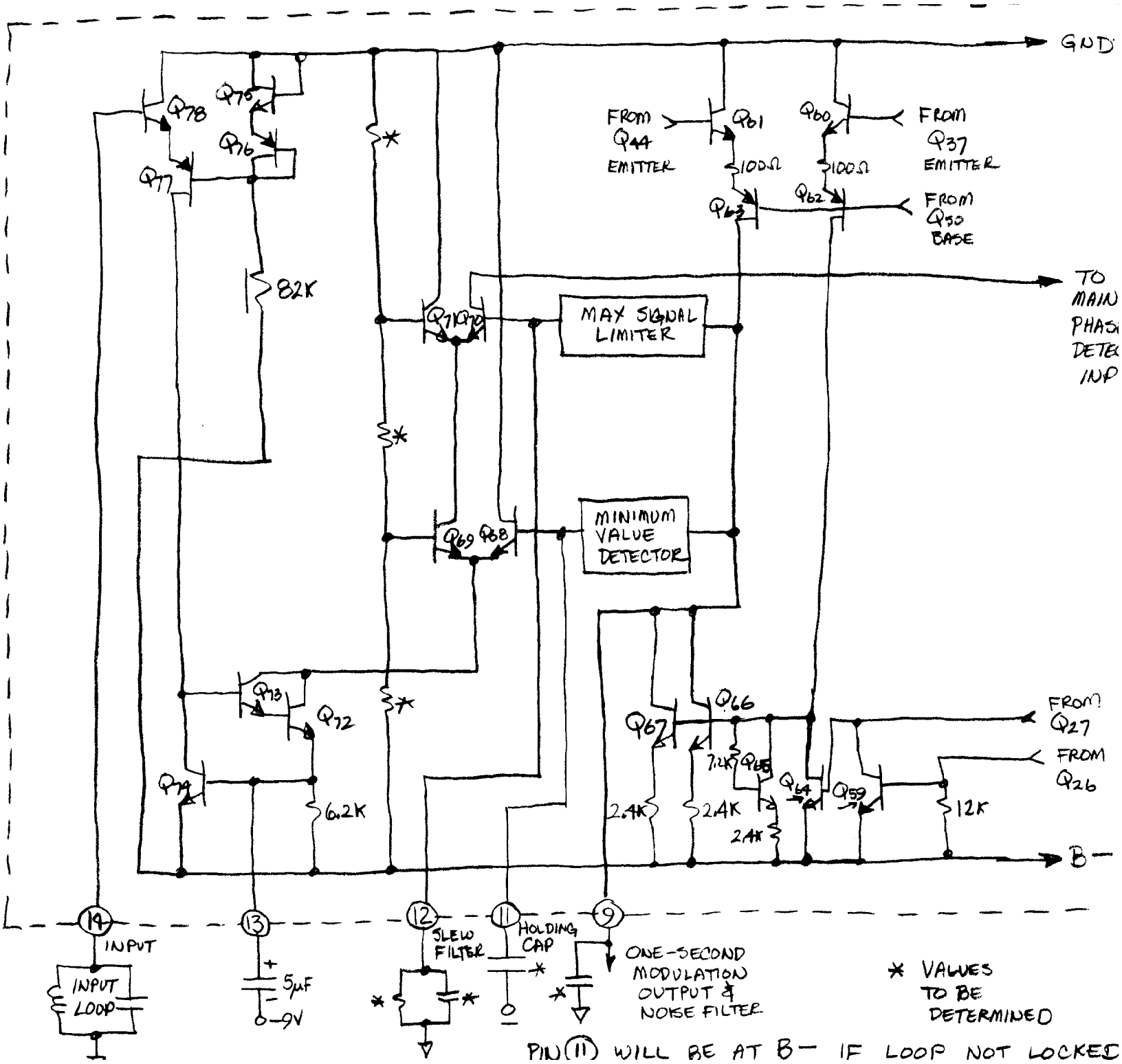
The input loop is comprised of 100 turns of #28 wire wound inside $\frac{1}{4}$" copper tubing for maximum electrostatic shielding - thus reception is by way of the transmitted electromagnetic component of the signal, this method eliminated some 60 dB of

noise pick-up when tested in the BOWMAR lab.

It is my opinion that the phase detector implementation is probably a patentable circuit. If the AGC is brought to fruition, the overall system is likely to be patentable. Perhaps Joe Roediger can give you his opinion on this.




GROUND
.1μF
BYPASS CAP.
60 KHz OUTPUT
I/C
B-
SUB.
FROM PREAMP
TO QUAD. DET
TO QUAD DET.
SCHEMATIC CONTINUED NEXT PAGE
INTERSTAGE TANK
.7 mH
.01μF
BYPASS CAP.
.1μF
CENTER FREQ. SET & LOOP COMP.
VCO CAP
.001μF
-9V
NBS RECEIVER
VCO & MAIN
PHASE DETECTION



NBS RECEIVER
PREAMP, AGC
&
SIGNAL OUTPUT
STAGES

WWVB CODE SEQUENCE

P = .8 SEC PULSE FOR FRAMING

"0" = .2 SEC PULSE

"1" = .5 SEC PULSE

U = UNCODED PULSE POSITION - GENERALLY A "0" (.2 SEC)

CODING:

P ← BEGIN MINUTE

P

40
20
10
U
8
4
2
1
} MINUTES SET

P

U
U
20
10
U
8
4
2
1
} HOURS SET

P

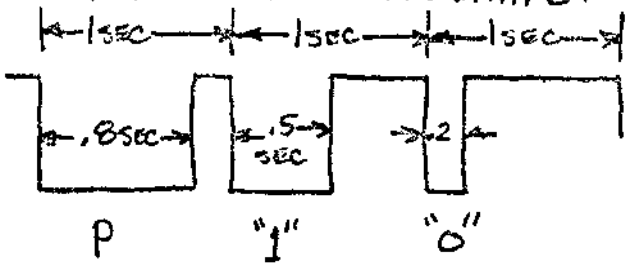
U
U
200
100
U
80
40
20
10
P
8
4
2
1
U
U
} DAYS SET

35 SEC ELAPSED TIME

} VTI CORRECTIONS

} TWO P'S OCCUR TOGETHER ONLY AT BEGINNING OF MINUTE AS SHOWN

EXAMPLE OF WAVESHAPE:



6/13/74

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