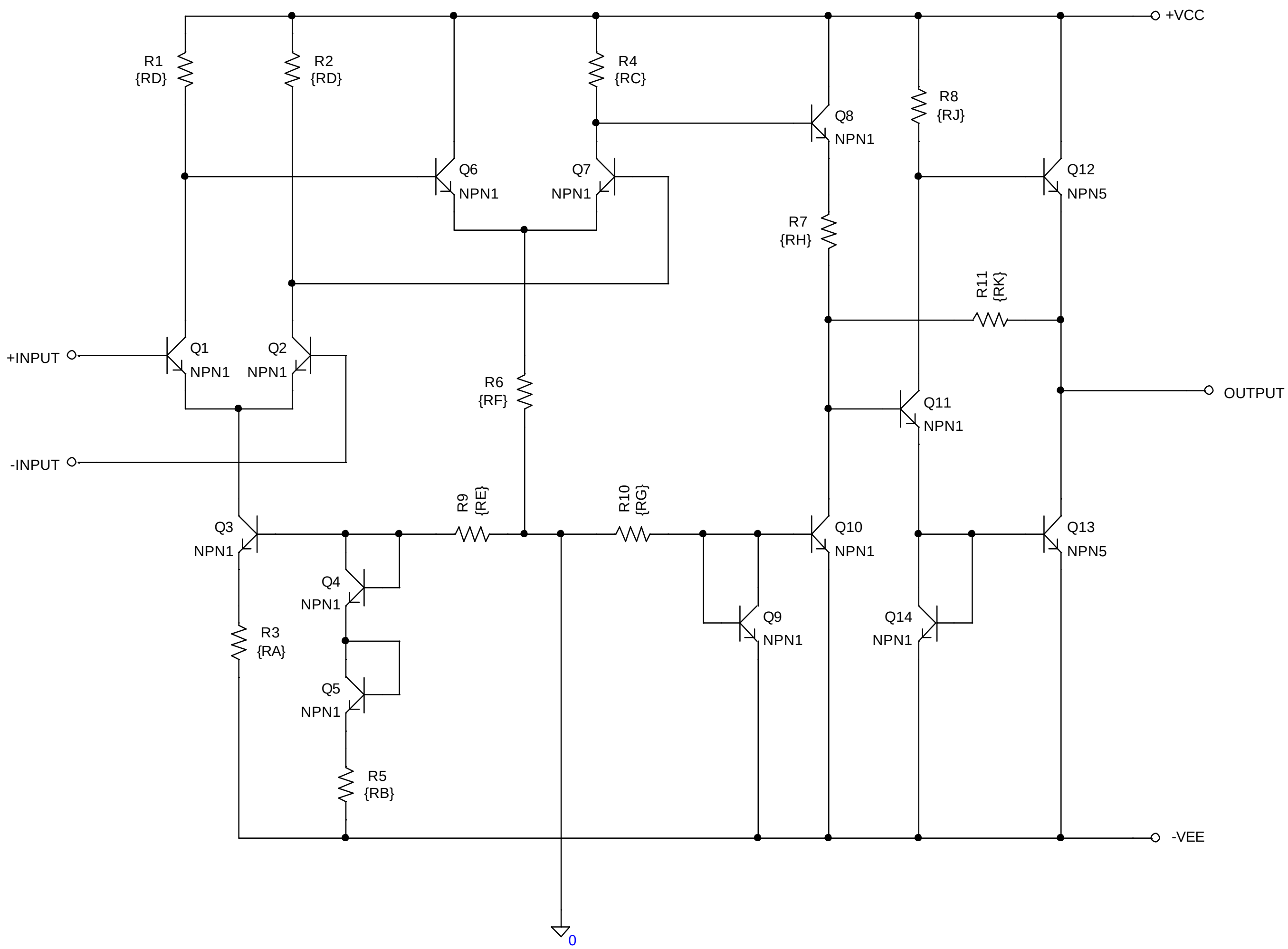

PARAMETERS:

RA	2.2K
RB	1.5K
RC	3K
RD	7.75K
RE	3.2K
RF	1.5K
RG	3.4K
RH	6K
RJ	5K
RK	30K

NOMINAL MC1530 SCHEMATIC

ANALOG INNOVATIONS, Inc.
824 E. CATHEDRAL ROCK DRIVE
PHOENIX, AZ 85048-6300
(480) 460-2350 FAX: (480) 460-2142

Title:
Analysis of MC1530 Bias Structures

Size	FileName:	REV
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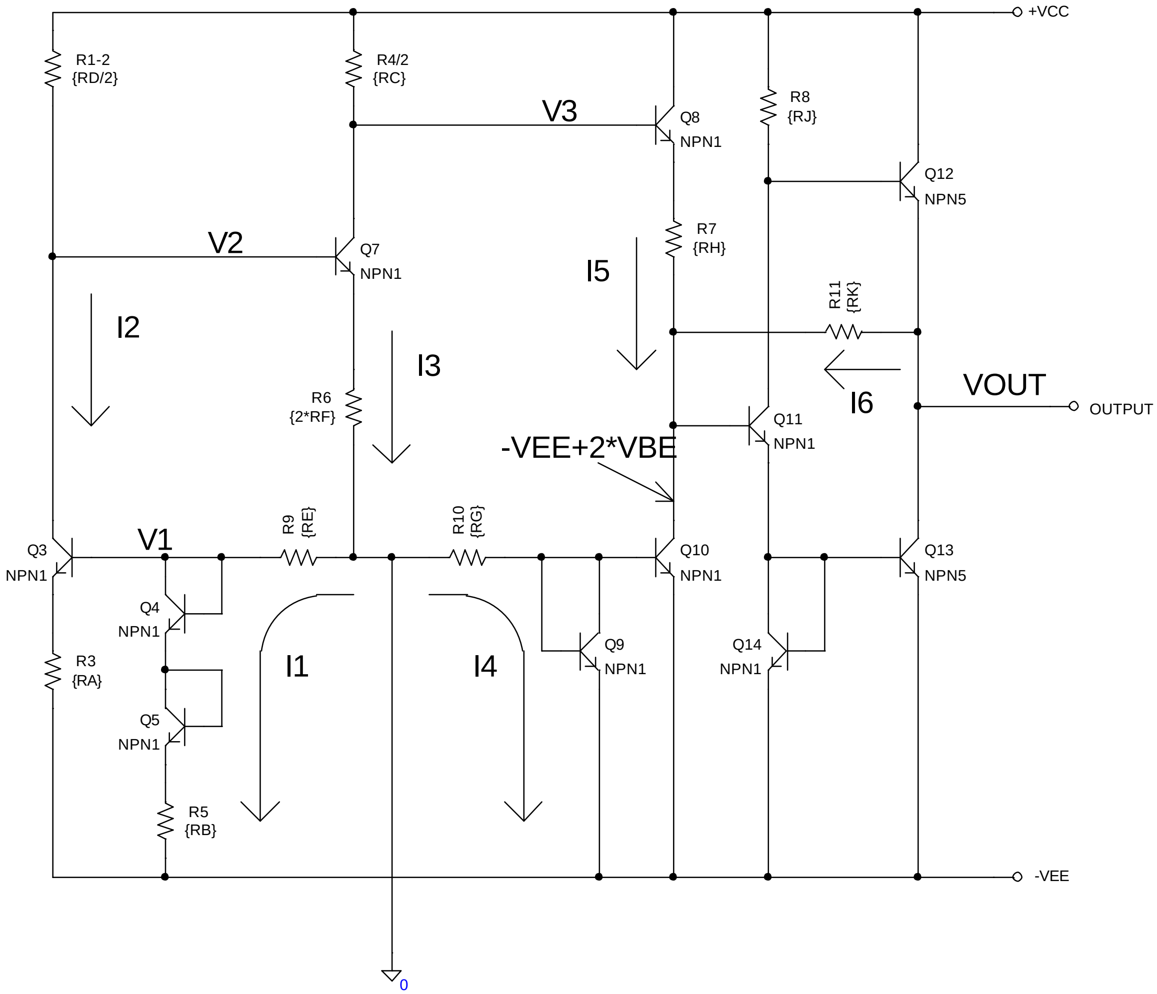
January 20, 2004, 1:58 PM

IF BOTH INPUTS ARE TIED TO GROUND THE CIRCUIT REDUCES TO:



PARAMETERS:	
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COMMON MODE MODEL
(Paralleled Devices Eliminated,
Q7 Current Proportioned)

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Size A | FileName: ...\MC1530-TeachingExercise.sch | REV A

January 20, 2004, 1:58 PM | Sheet 2 of 2

I1 = (VEE - 2*VBE)/(RB + RE)
V1 + VEE = I1*RB + 2*VBE
I2 = (I1*RB + VBE)/RA
V2 = VCC – I2*RD/2
I3 = (V2 – VBE)/(2*RF)
V3 = VCC – I3*RC
V3 = VCC – (V2 – VBE)*RC/(2*RF)
V3 = VCC – (VCC – I2*RD/2 – VBE)*RC/(2*RF)

Observing the schematic we can see that no more terms in VCC will be introduced as we progress through the circuit, so now would be a good time to eliminate VCC from our equations. Let’s choose 2*RF = RC

Then:

V3 = I2*RD/2 + VBE
V3 = (I1*RB + VBE)*RD/(2*RA) + VBE
V3 = ((VEE – 2*VBE)*RB/(RB + RE) + VBE)*RD/(2*RA) + VBE
I5 = (V3 – 3*VBE + VEE)/RH
I6 = (VOUT – 2*VBE + VEE)/RK
I4 = (VEE –VBE)/RG

But (in the linear operating region):

I4 = I5 + I6

Thus:

(VEE – VBE)/RG = (V3 – 3*VBE + VEE)/RH + (VOUT – 2*VBE +VEE)/RK

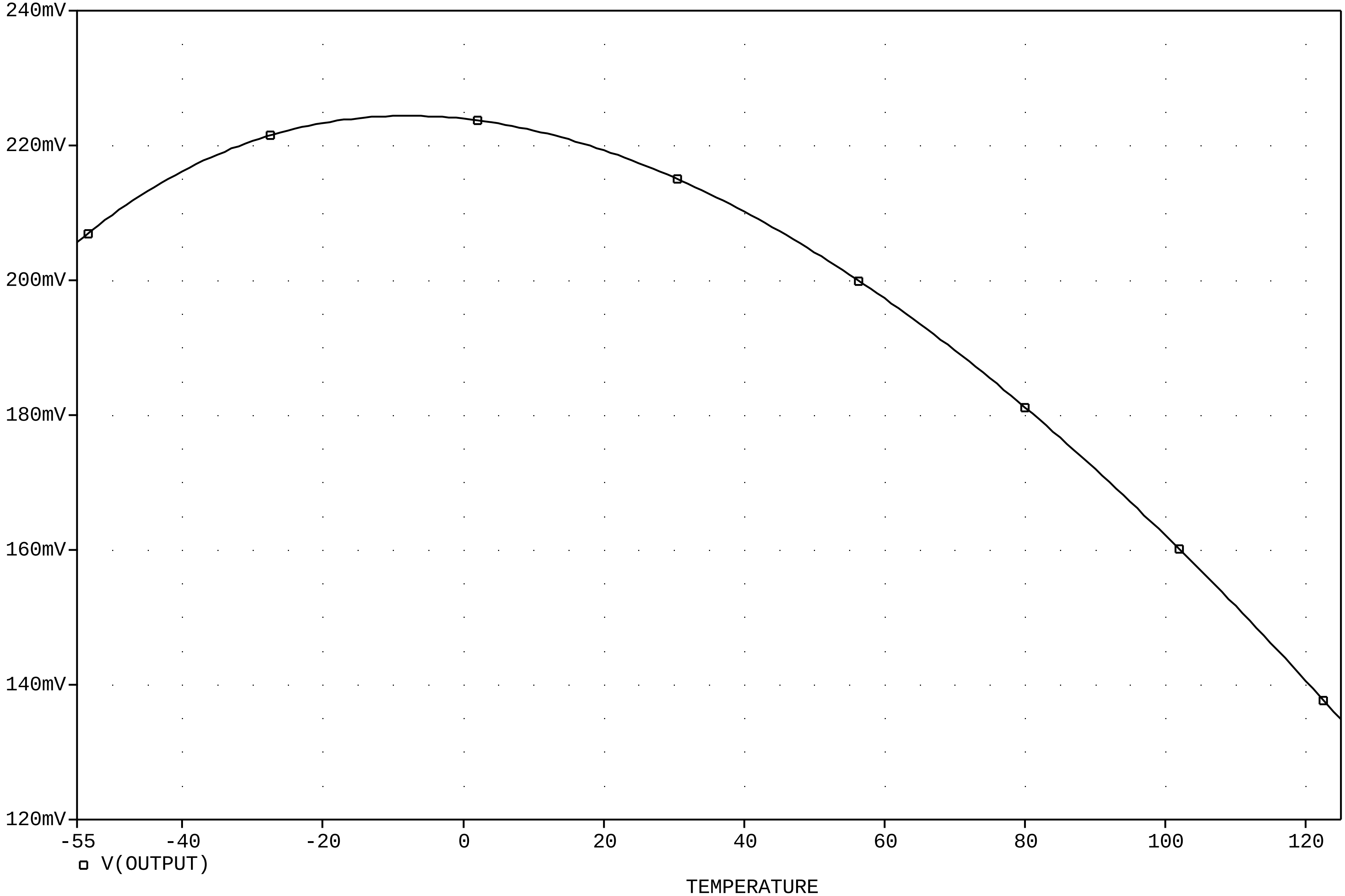
(VEE – VBE)*RK/RG = RK/RH*(((VEE – 2*VBE)*RB/(RB + RE) + VBE)*RD/(2*RA) – 2*VBE +VEE) + VOUT –2*VBE + VEE

VOUT = VEE*(-1 + RK/RG – RK/RH*(RB/(RB + RE)*RD/(2*RA) + 1))
+ VBE*(-RK/RG –RK/RH*((-2*RB)/(RB + RE) + 1)*RD/(2*RA) –2) +2)

Substituting Values…

VOUT = 0 (Independent of VCC, VEE and VBE, within the ratio accuracies attainable on-chip)

MC1530-TeachingExercise Simulated with 2N3904's



Analog Innovations, Inc.
824 E. Cathedral Rock Drive
Phoenix, AZ 85048-6300
(480)460-2350

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DISCUSSION

The MC1530 OpAmp Chip was designed pretty much as outlined in the above analysis EXCEPT that I worked the equations backwards from the desired output voltage with some judicious application of experience. Clearly the design methodology must keep track of the allowable signal swings at various points within the circuit and an eye must be kept on maintaining a reasonable common-mode range at the input.

This OpAmp design was the fastest and had the highest gain-bandwidth product (GBW) of its day (1965). It is STILL manufactured (Lansdale bought the product rights from Motorola a few years ago).

Not obvious, but the output stage is SLIDING CLASS-A (note the 5X output devices), thus there is no crossover distortion.

Specifications:

Power	±9V (absolute max), Specs at ±6V Bias:
I(quiescent)	±9.2mA Typical
ILOAD	±10mA
Output	±5V into 1K
DC Gain	>4500 (73dB)
GBW	>10MHz
Slew Rate	Up to 33V/µsec depending upon feedback configuration
VOS	±1mV Typical
Input Bias	3µA Typical (MC1530), 25nA Typical (MC1531)
Input Z	15K Typical (MC1530), 600K Typical (MC1531)
Output Z	25 Ω Typical
CM Range	±2V Minimum
CMRR	75dB Typical
PSRR	80dB Typical

LAYOUT:

I did the layout of this chip myself, on a quadrille pad. I also cut the Rubylith to make the mask set.

A photo of the chip is on the next page...