LM195
PROTECTED POWER TRANSISTOR

ICE Publication 10503-11

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LM195
PROTECTED POWER TRANSISTOR

The LM195 is a darlington power transistor manufactured in a linear I/C process so that various protective circuit elements may be included on the same chip. A simplified block diagram of the circuit is shown in Figure 1.

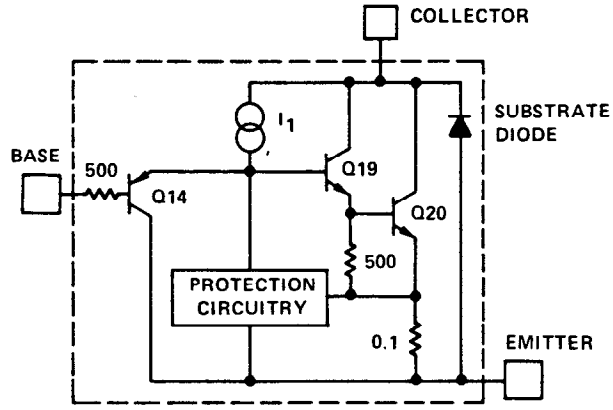


Figure 1. Simplified Circuit if the LM195

Transistors Q19 and Q20 comprise the actual power device. Q14 serves as a buffer for the base drive so that the input may be grounded at turn-off. The substrate diode is a natural occurrence of the process and serves as reverse current protection. The 0.1Ω resistor senses current and provides one input to the protection circuitry to provide short-circuit protection. Other inputs to the protection circuitry are collector voltage, saturation condition, and temperature sensing. Thus, through proper circuit configuring, power limiting and thermal shut-down are provided.

The published schematic is as shown in Figure 2. The actual circuit has been determined, by tracing the actual die construction, to be that shown in Figure 3. The differences may be noted as follows:

R_B represents the drop due to ballast resistors
Q5 has two emitters.
Q11 has ten emitters.
R3, R4, R5 values are different from published values.
R23 does not exist.
C2 has been added for loop stability
Q20 has multiple emitter structures.
D4 is not a simple diode structure.
Q17/Q18 are in a shared island.

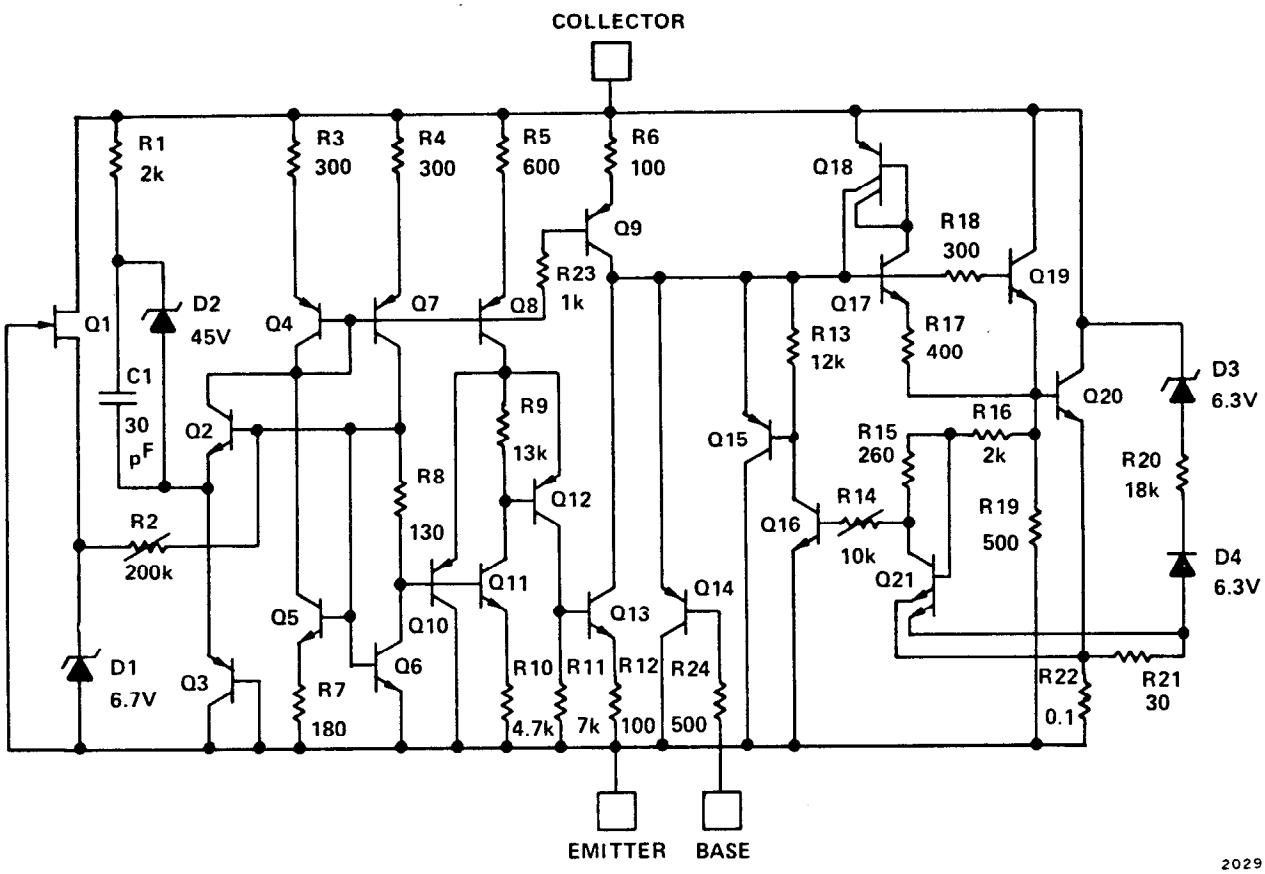


Figure 2. Published Schematic Diagram of the LM195

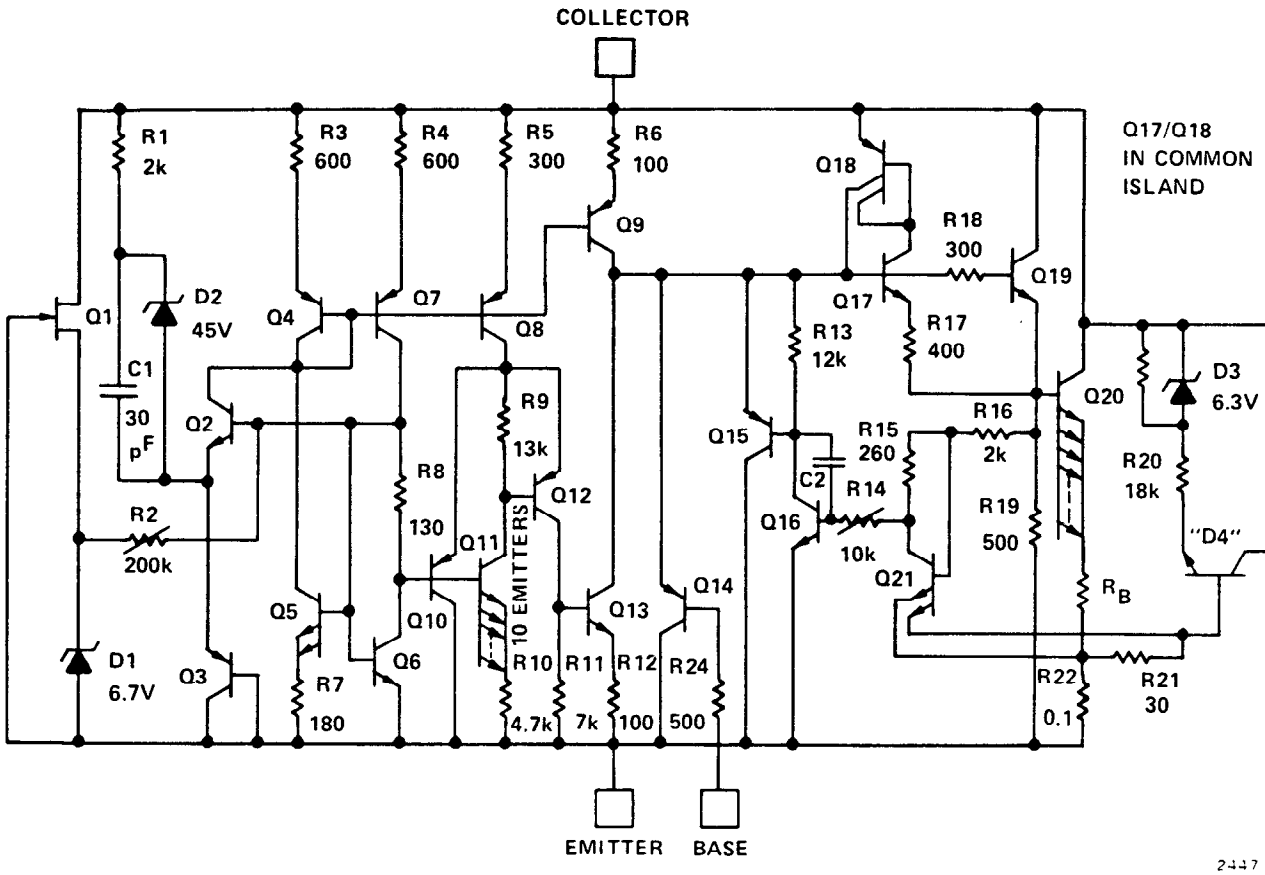
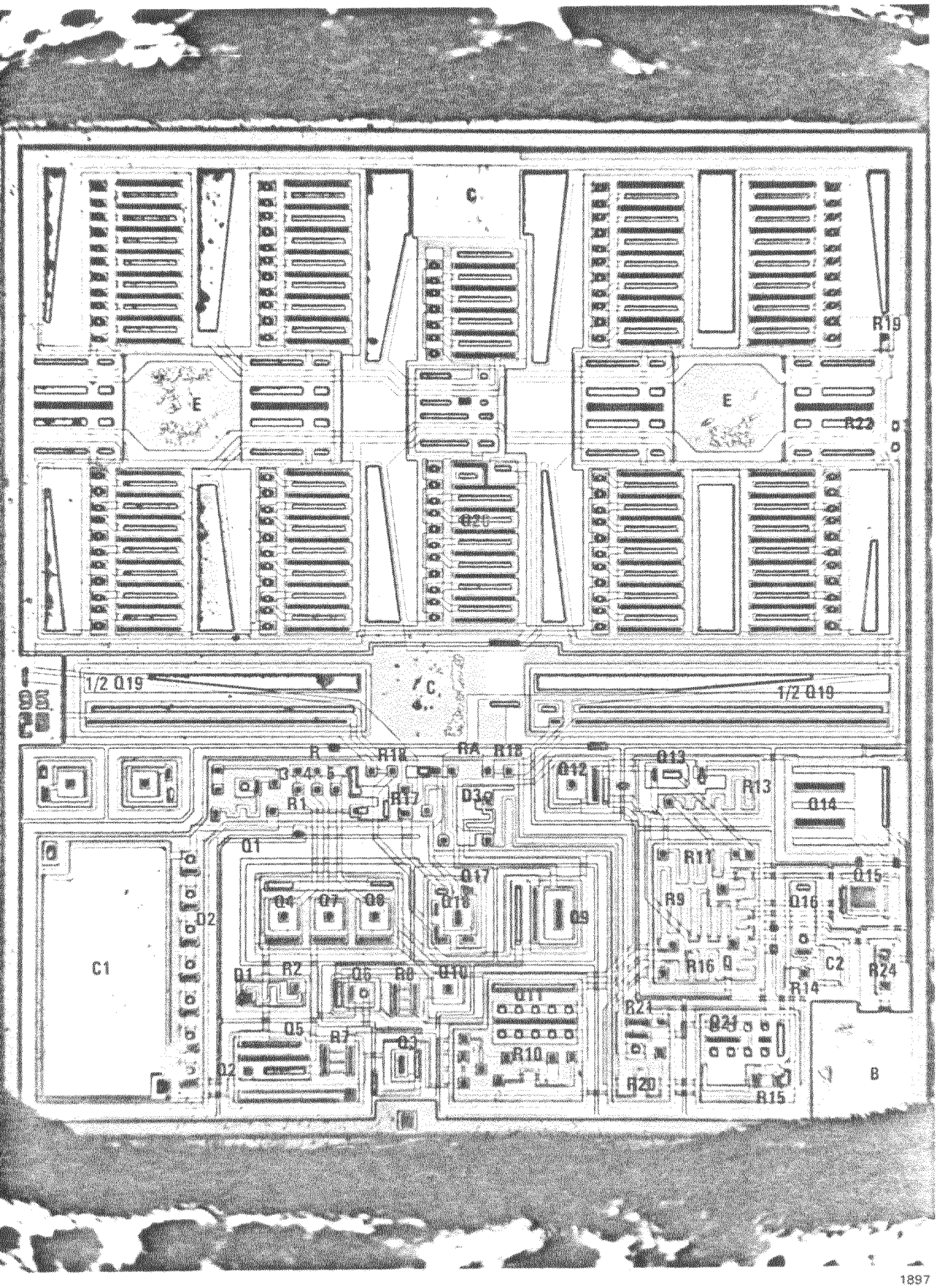
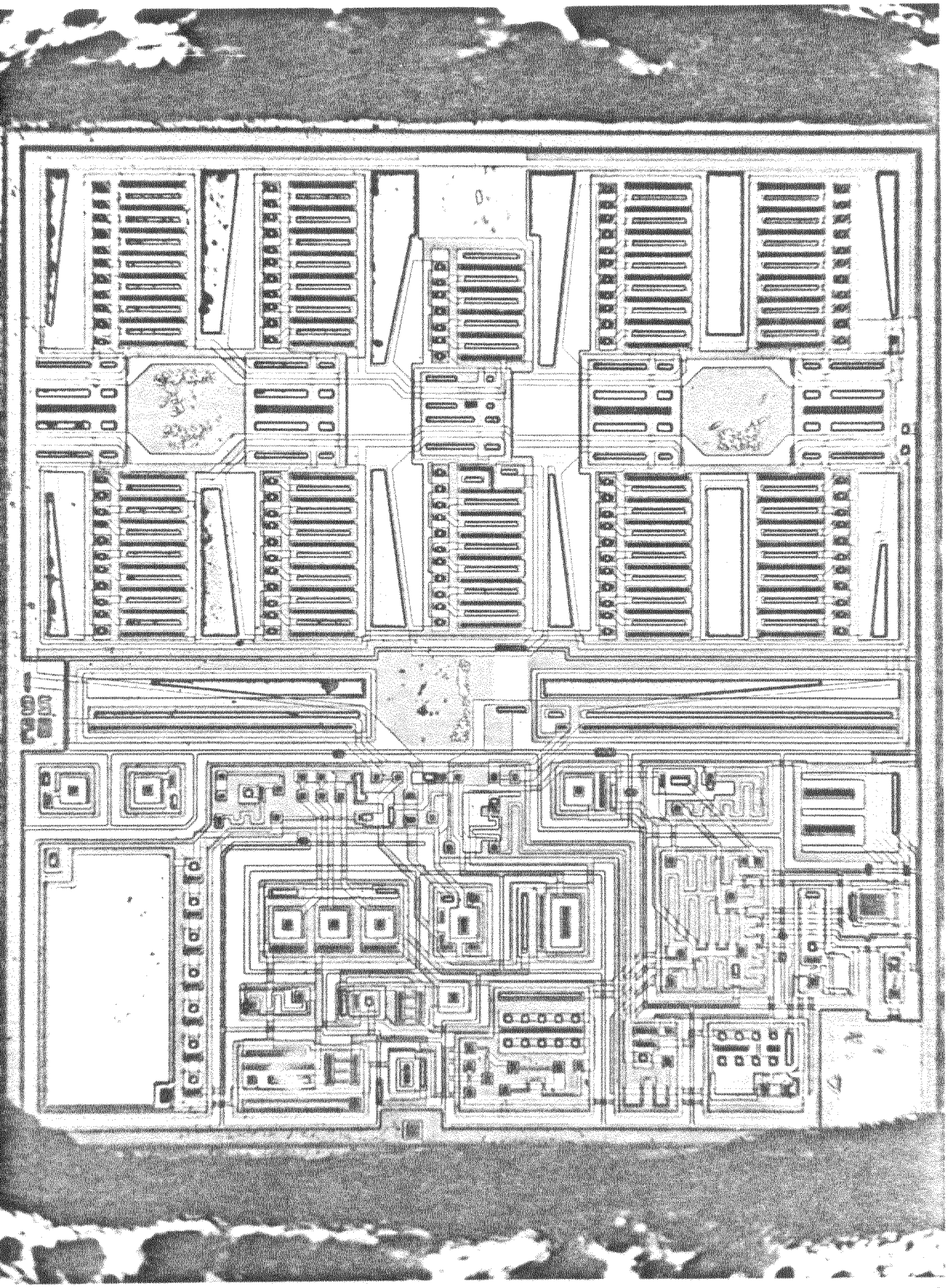
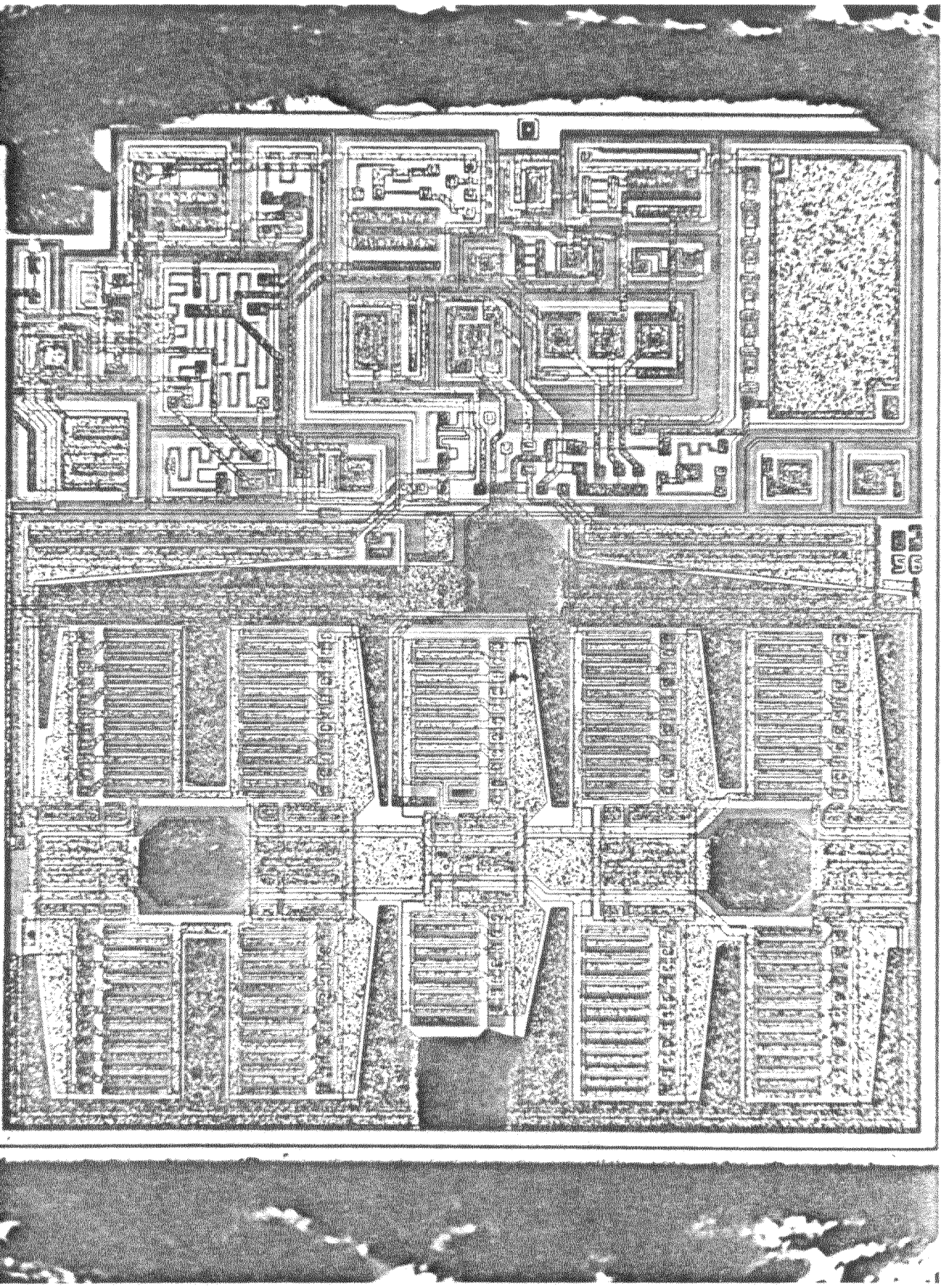


Figure 3. Actual Schematic Diagram of the LM195

The die photo with metal removed is shown with overlaid designators in Figure on page 4. Figure 5 shows the die photo with metal. Figure 6 shows the detail view of one section of the output device Q20. Note the interleaving of base and emitter stripes and the ballasting emitter resistors to balance current. Figure 7 shows the construction of Q17 and Q18, an NPN and a PNP sharing the same isolation island, which you might otherwise have trouble locating.


C
E
E
R19
R22
1/2 Q19
1/2 Q19
R
R18
R16
R1
R17
D30
Q12
Q13
R13
Q14
Q1
Q17
Q4
Q7
Q8
Q16
Q9
R11
Q15
R9
D16
C1
Q2
Q1
R2
Q6
R8
Q10
Q11
R16
C2
R24
R14
R21
Q5
R7
Q3
R10
R20
R15
B





1899

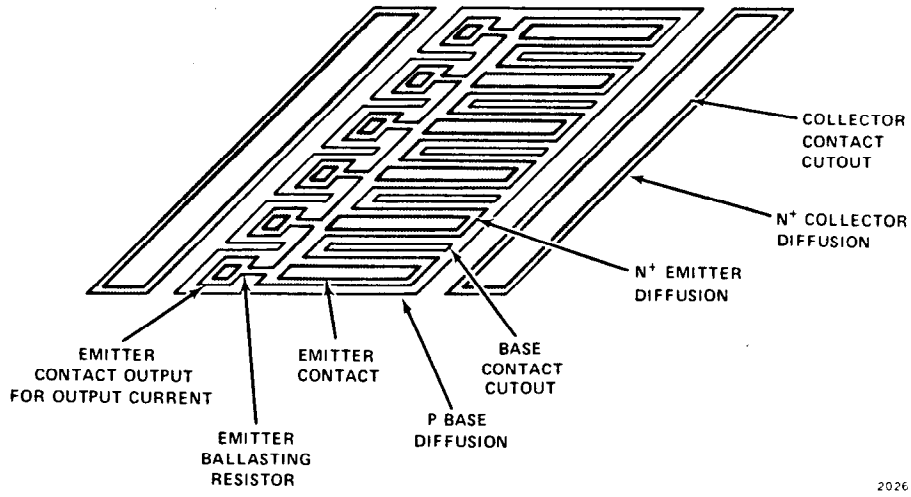


Figure 6. Detailed Structure of One Section of the Power Transistor

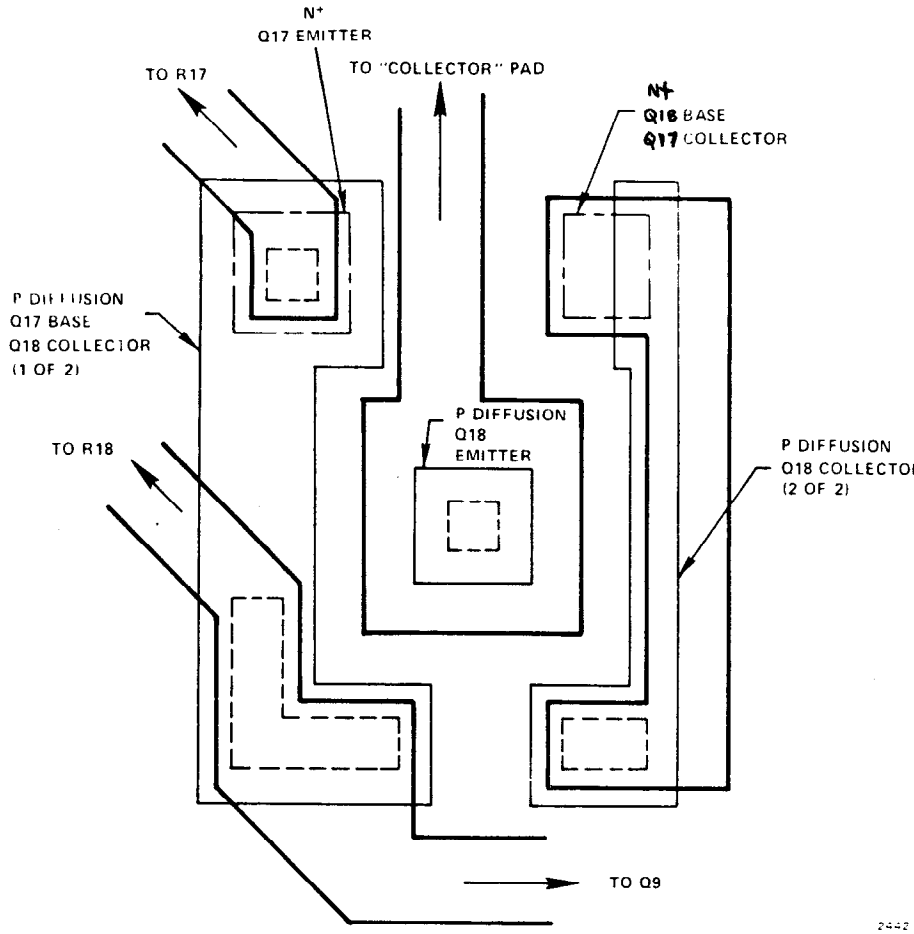


Figure 7. Construction of Q17 and Q18

THE CIRCUIT DESIGN AND RESULTING PERFORMANCE

Now that we have examined the physical structure of the LM195, let us analyze the circuit design to understand its operation.

Reference Bias System

As with most I/C designs, the performance of the LM195 revolves about a reference bias system. This reference is comprised principally of Q4, Q5, Q6 and Q7 (see Figure 8).

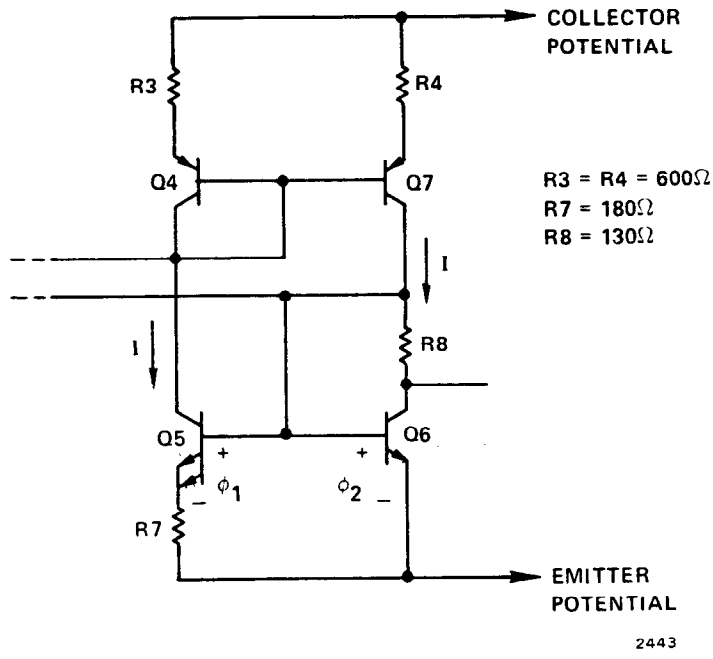


Figure 8. Reference Bias Schematic

Since R3 = R4, the current, I, appears in both legs equally. Q5 has two emitters versus one for Q6, thus

$$\phi_2 - \phi_1 = \frac{kT}{q} \ln 2 = IR_7. \qquad (1)$$

That is, a reference current has been established of value

$$I = \frac{kT}{qR_7} \ln 2. \qquad (2)$$

Any PNP current sources biased from the same base rail as Q4 and Q7 will thus have a proportionate current. In the LM195 these are Q8 (at twice reference current) and Q9 (at approximately 5-6 times reference current).

You will have probably noted that equation (2) relates a current unrestrained by the outside world. This "desensitization" to power supplies

is a very desirable feature, allowing circuit performance to be specified without regard to outside variables. However, as with any reference of this sort, we must "start" it (cause an initial flow of current) so that equilibrium can be attained. In the LM195 this is accomplished with Q1, D1 and R2 (see Figure 9). Q1 is a pinched EPI resistor FET driving current through R2 (an emitter pinched base resistor) into the base of Q6 to initiate current flow.

Once current flow begins, the loop advances the current level until equilibrium is reached ($\approx 100\mu A$ at 25°C). Diode D1 limits the level of start-up current so that collector voltage has an insignificant effect on the reference level.

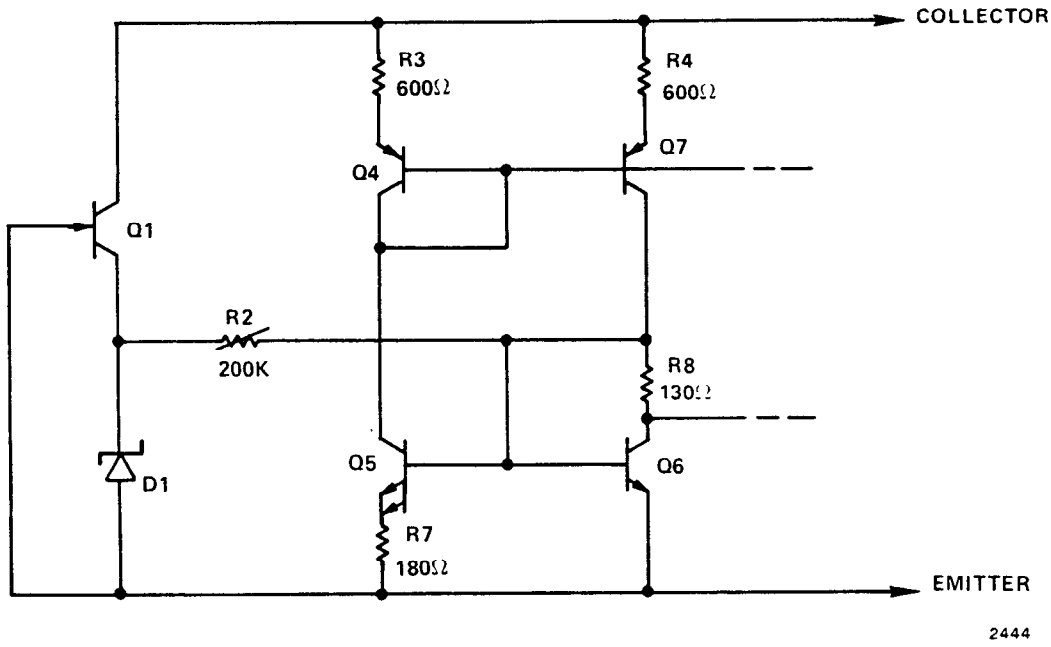


Figure 9. Reference Bias Schematic

Thermal Shutdown

You will note from Figure 3 that if we can divert the current drive from the base of Q19 we can effectively shut off all current flow in the output device. It would be desirable to do this at some temperature level lower than that temperature at which junction degradation begins. Since temperature sensing is related to the reference bias, let us examine this circuitry next. Observe the circuit arrangement of Figure 10.

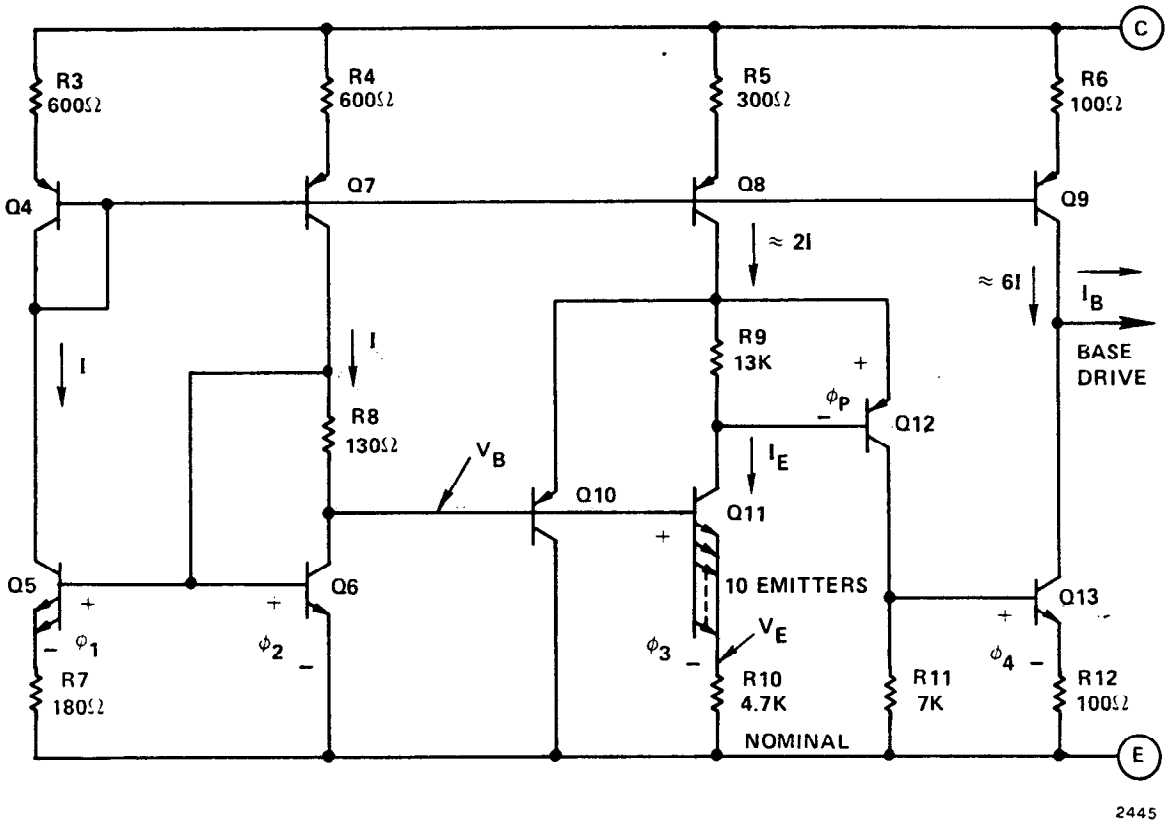


Figure 10. Thermal Shutdown Schematic

In general terms one can observe that the voltage on R10 (V_E) slowly rises with temperature, increasing the current through R10 and thus through R9, such that at a critical temperature Q12 thresholds, turns on Q13 and removes the base drive to the output. Let us now compute the critical temperature. Recall that

$$I = \frac{kT}{qR_7} \ln 2 \tag{2}$$

then

$$V_B = \phi_2 - IR_8 \tag{3}$$

or

$$V_B = \phi_2 - \frac{R_8}{R_7}\frac{kT}{q} \ln 2. \tag{4}$$

Then

$$V_E = V_B - \phi_3 \tag{5}$$

or

$$V_E = \phi_2 - \phi_3 - \frac{R_8}{R_7}\frac{kT}{q} \ln 2. \tag{6}$$

But

$$\phi_2 = \frac{kT}{q} \ell_n \frac{I}{I_S} \tag{7}$$

and

$$\phi_3 = \frac{kT}{q} \ell_n \frac{I_E}{10I_S} \tag{8}$$

since Q11 has 10 emitters.

Thus

$$\phi_2 - \phi_3 = \frac{kT}{q} \ell_n \frac{10I}{I_E}, \tag{9}$$

and

$$V_E = \frac{kT}{q} \ell_n \frac{10I}{I_E} - \frac{R_8}{R_7} \frac{kT}{q} \ell_n 2. \tag{10}$$

Since $R_8 < R_7$ equation (10) represents a net positive temperature coefficient for V_E, and I_E is given by

$$I_E = \frac{V_E}{R_{10}} = \frac{kT}{qR_{10}} \left[\ell_n \frac{10I}{I_E} - \frac{R_8}{R_7} \ell_n 2 \right]. \tag{11}$$

Because I and I_E are themselves functions of temperature, equation (11) is transcendental in I_E and thus is impossible to solve in closed form. Since we know that qualitatively I_E varies with temperature as desired (and we are "reverse engineering" the design anyway) let us turn (11) around, assume some educated values for I and I_E and solve for R10. Equation (11) then becomes

$$R_{10} = \frac{kT}{qI_E} \left[\ell_n \frac{10I}{I_E} - \frac{R_8}{R_7} \ell_n 2 \right]. \tag{12}$$

Since we are always dealing (in a good I/C design) only with resistor ratios we shall ignore TCR (what effects remain will be only second order logarithmic ΔV_{BE}'s).

Let us assume a critical shutdown temperature of 175°C (448°K), then from (2) we have

$$\frac{kT}{q} = .026 \text{ at } 25°C = 298°K$$

$$I = .026 \frac{448}{298} \cdot \frac{1}{180} \ell_n 2 = 150\ \mu A \tag{13}$$

Determining I_E is a somewhat more approximate problem (and one of the design defects of this thermal shutdown). We may estimate ϕ_P and thus I_E at threshold as follows:

.700	ϕ_P at 100μA at 25°C (typical for process)
−.300	−2mV/°C × 150°C rise
.400	ϕ_P at 100μA @ 175°C
−.027	estimate transistor current at threshold to be 50μA $\left(-\frac{kT}{q}\ell_n 2\right)$
.373	estimated ϕ_P at 50μA at 175°C.

Thus

$$I_E = \frac{\phi_P}{R_9} = \frac{.373}{13K} = 28.6\mu A. \qquad (14)$$

Then calculate

$$R_{10} = \frac{.026(448)}{28.6 \times 10^{-6}(298)} \left[\ell_n \frac{10(150)}{28.6} - \frac{130}{180}\ell_n 2\right]$$

$$R_{10} = 4.728K. \qquad (15)$$

The reader will observe from the die photo that R10 has many metalization taps to allow "tweeking" of this value to overcome the inaccuracies in estimating process variables.

A desirable feature, not included in this design, would have been a slight amount of hysteresis to give a sharp turn-off at the critical temperature, thus avoiding any coincident safe-area problems at shutdown.

Power Handling Drives and Protection

Now consider the circuitry of Figure 11.

Q14 by virtue of the potential at the "base" B controls the amount of drive current entering Q19 and thus the drive to Q20. Thus behavior is that of a compound darlington transistor under normal operating conditions.

In saturation Q18 provides additional base drive to Q19 in a novel fashion. When the collector is in saturation, β of Q19 falls and the base current (in R18) increases. Since Q17 and R17 are in parallel with Q19 and R18, the current to Q18 increases, increasing the output current from the collector of Q18. This approach ensures firm saturation by accomodating the need for a forced β at saturation. At other load conditions the contribution of Q18 is negligible (note that 300/400 = .75 < 1, so no latch-up can occur).

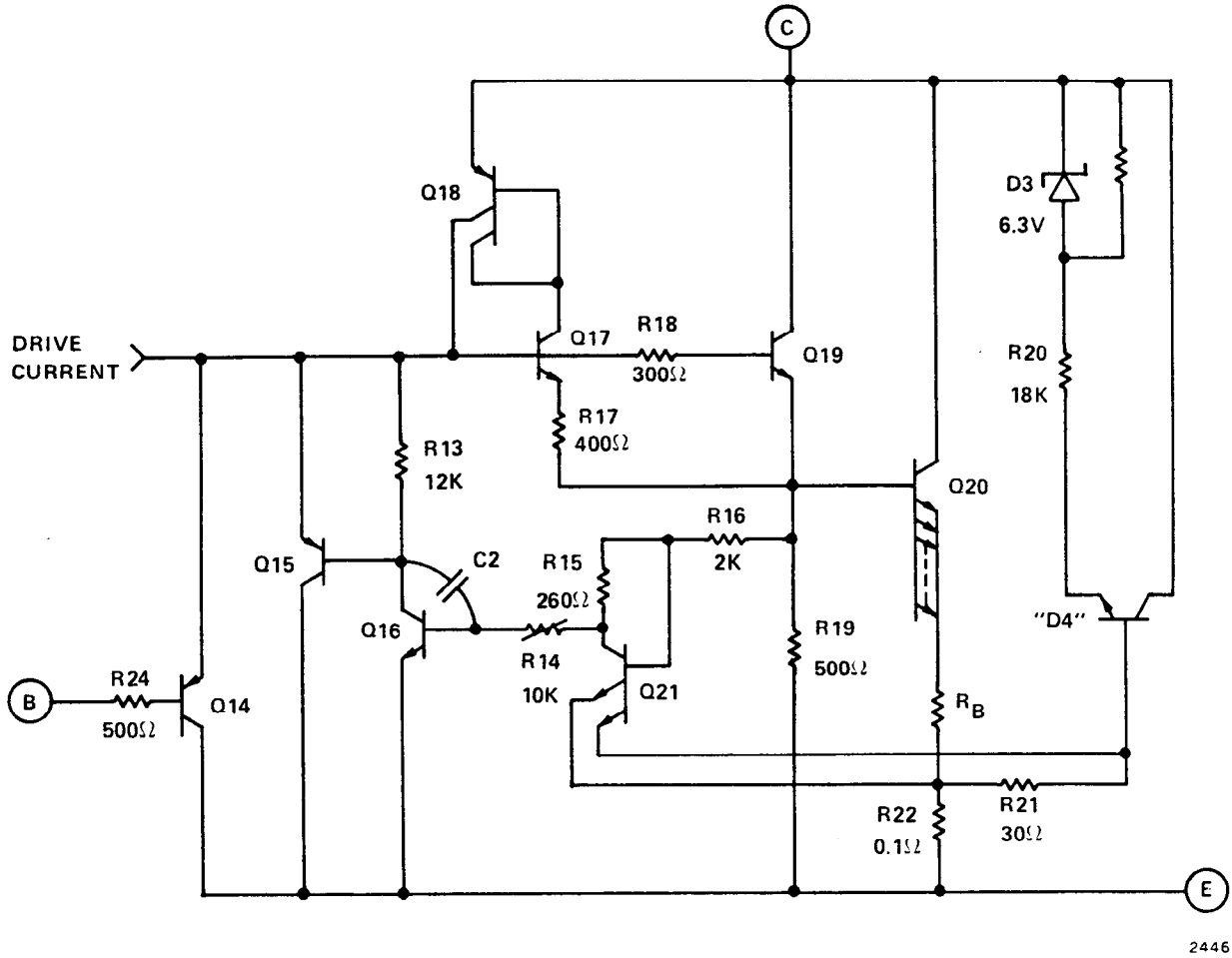


Figure 11. Power Handling Drive and Protection Schematic

Short circuit protection is accomplished using sense resistor R22 (see Figure 11) and level shifting the resultant voltage drop through Q21 to the base of Q16. When Q16 thresholds, Q15 conducts drawing base drive away from Q19. (Current limit occurs at approximately 2 amps at 25°C.) Above approximately 12.6 volts, D3 and D4 conduct and add a voltage term to the sense potential reducing the current level at which limiting occurs, thus providing a semblance of power limiting. (Remember, if the chip heats up, thermal shut-down will occur.) "Pole-splitting capacitor" C2 stabilizes the feedback loop during current limiting.

Special Feature

Turn-on time of a transistor with substantial current gain but limited drive will be restrained by Miller-effect capacitance. Since this is a substantial effect in a darlington structure, R1, C1, D2, Q2 and Q3 have been added (see Figure 3.) During negative-going slew conditions Q2 is forced into conduction, increasing Q4's current and thus the available base drive during the transition. Once saturation is reached this extra drive ceases. D2 limits voltage on C1. Q3 limits reverse potential application on base-emitter of Q2.

PUBLICATION 10503-25

REVIEW OF LM117

ADJUSTABLE VOLTAGE REGULATOR

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PUBLICATION 10503-25

REVIEW OF LM117 ADJUSTABLE VOLTAGE REGULATOR

The LM117 Adjustable Voltage Regulator is an example of an IC design that yields two circuit varieties from one mask set simply by using metallization options. For example, examine Figure 1, the published LM195 schematic, and then compare to Figure 2, the published LM117 schematic.

Note that the only significant difference between the two schematics is the mid-section of the LM117 where voltage regulation control circuitry has been added. (The devices exist on the LM195, only a metal mask change now connects them into the system.)

A little observation will easily convince you that Q_{16}, Q_{17}, Q_{18} and Q_{19} form a variation of a band-gap reference and that Q_{12}, Q_{13} and Q_{15} buffer its output so that the reference can drive the base of the output devices (Q_{25} and Q_{26}).

The band-gap reference is novel in some aspects and warrants analysis.

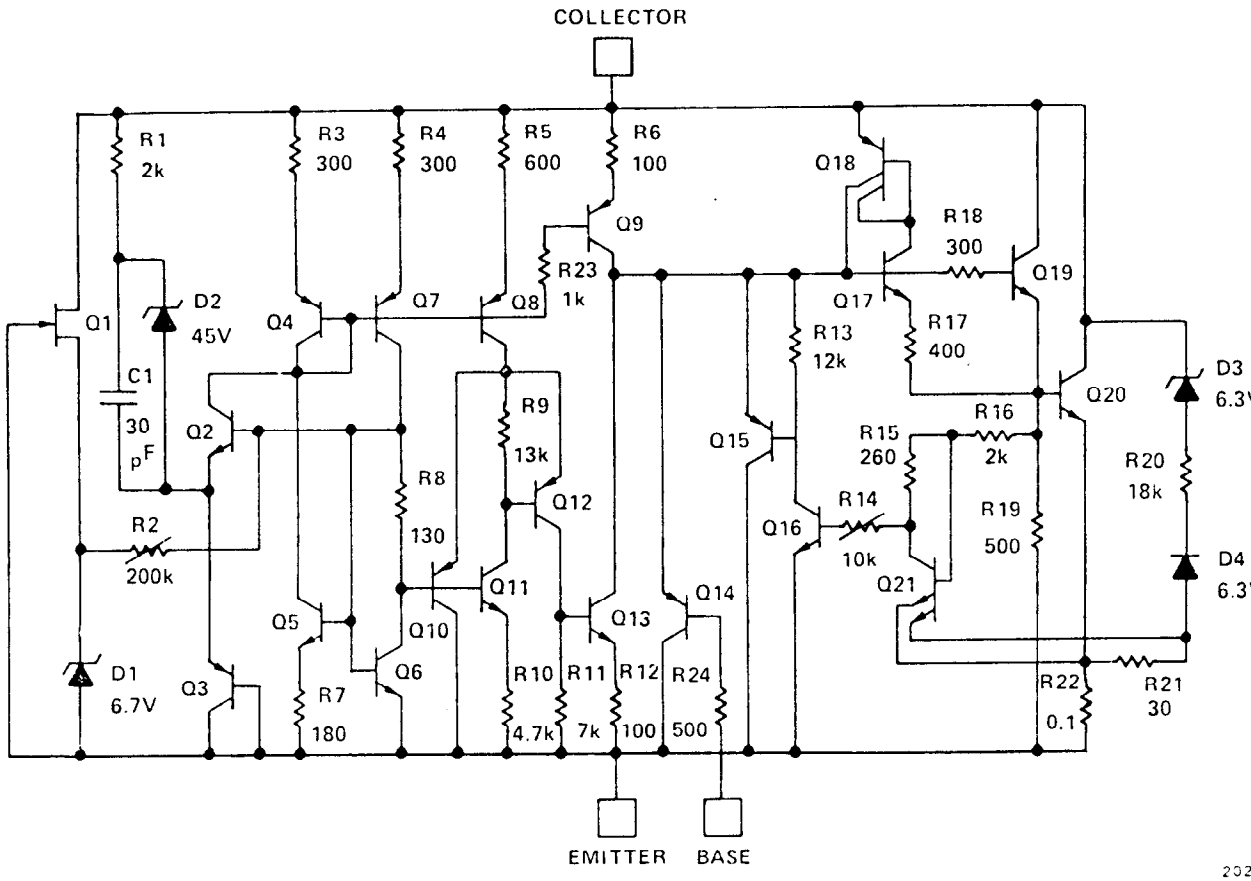


Figure 2. Published Schematic Diagram of the LM195

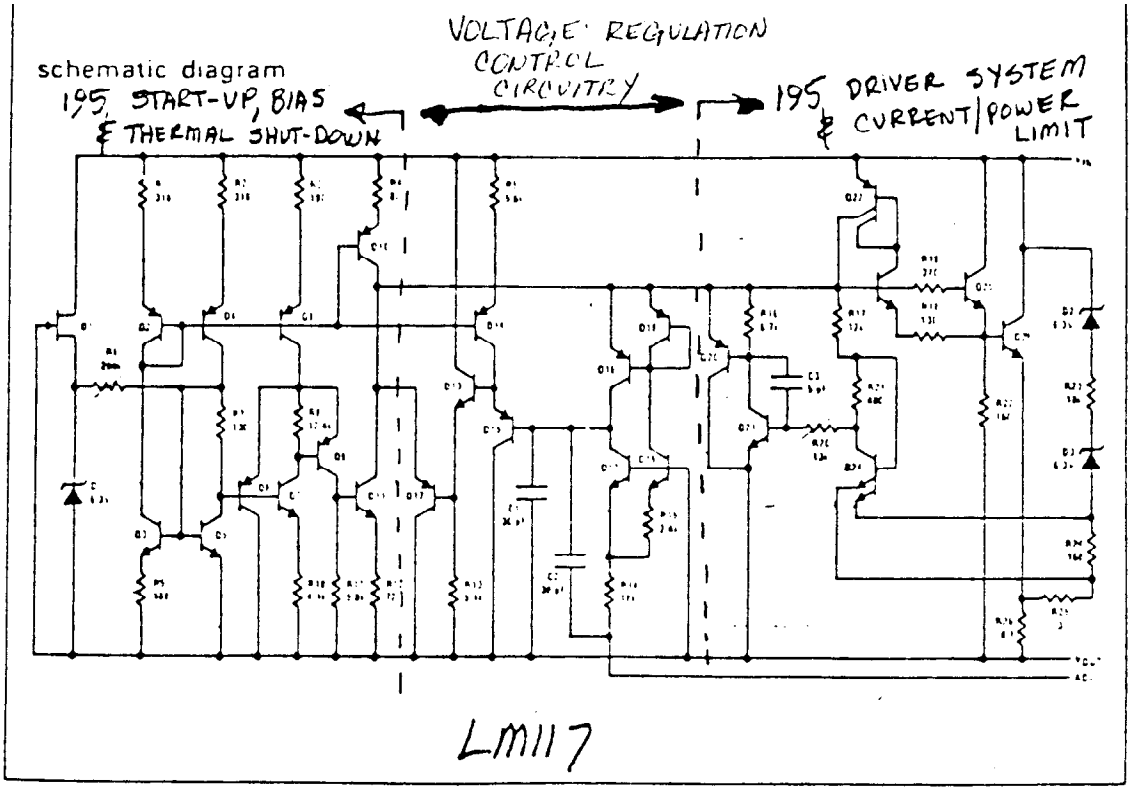

schematic diagram
VOLTAGE REGULATION CONTROL CIRCUITRY
195 START-UP, BIAS & THERMAL SHUT-DOWN
195 DRIVER SYSTEM & CURRENT/POWER LIMIT
LM117

FIGURE 2.

Refer now to Figure 3. Q_{16} and Q_{18} must both have current level I since these devices comprise a 1:1 current mirror. We must now compute the conditions required of V_{out} and V_{adj} such that Q_{17} and Q_{19} run at current level I (balance and regulation is attained).

Utilizing the standard diode equations we obtain:

$$\emptyset_1 = \frac{kT}{q} \ln \frac{I}{I_S} \qquad (1)$$

$$\emptyset_2 = \frac{kT}{q} \ln \frac{I}{NI_S} \qquad (2)$$

$$\emptyset_1 - \emptyset_2 = \frac{kT}{q} \ln N = IR_E \qquad (3)$$

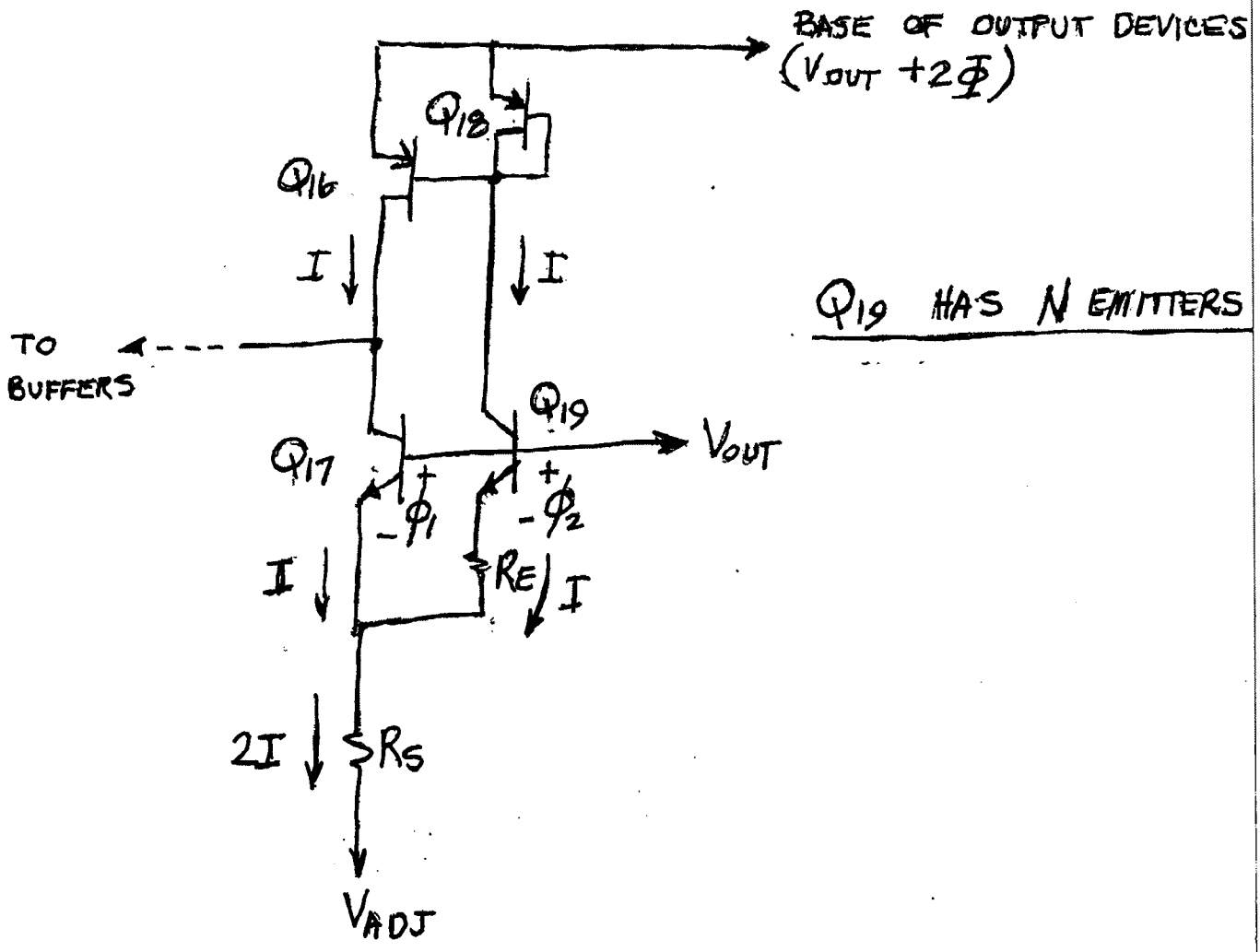
Thus we know immediately that the relative current densities in the emitters of Q_{17} and Q_{19} are in the ratio N.

We also note that

$$V_{OUT} - V_{ADJ} = \emptyset_1 + 2I_{RS} \qquad (4)$$

But from (3) we can compute:

$$I = \frac{1}{R_E} \frac{kT}{q} \ln N \qquad (5)$$



LM117 BAND-GAP

FIGURE 3.

Then:

$$V_{OUT} - V_{ADJ} = \emptyset_1 + \frac{2kT}{q} \frac{Rs}{R_E} \ln N. \qquad (6)$$

If we define $V_{OUT} - V_{ADJ} = V_{REF}$ we obtain:

$$V_{REF} = \emptyset_1 + \frac{2kT}{q} \frac{Rs}{R_E} \ln N. \qquad (7)$$

In a regulator, it is desirable that V_{REF} have zero temperature coefficient. Differentiating V_{REF} with respect to T and setting the result equal to zero we obtain:

$$0 = \frac{dV_{REF}}{dT} = \frac{d\emptyset_1}{dT} + 2 \frac{k}{q} \frac{Rs}{R_E} \ln N \qquad (8)$$

Since $\frac{d\emptyset_1}{dT}$ is known as

$$\frac{d\emptyset_1}{dT} = -2mV/°C \qquad (9)$$

and Rs and RE are given (on the schematic)

$$Rs = 12K$$

$$Re = 2.4K \qquad (10)$$

we obtain

$$N = 10 \qquad (11)$$

Then V_{REF} is given by

$$V_{REF} = \emptyset_1 + 10 \frac{kT}{q} \ln 10 \qquad (12)$$

with

$$\emptyset = .65 \text{ volts}$$

$$\frac{kT}{q} = .026 \text{ volts} \qquad (13)$$

we obtain

$$V_{REF} = 1.2487 = 1.25 \text{ volts} \qquad (14)$$

(The median value given by the data sheet)

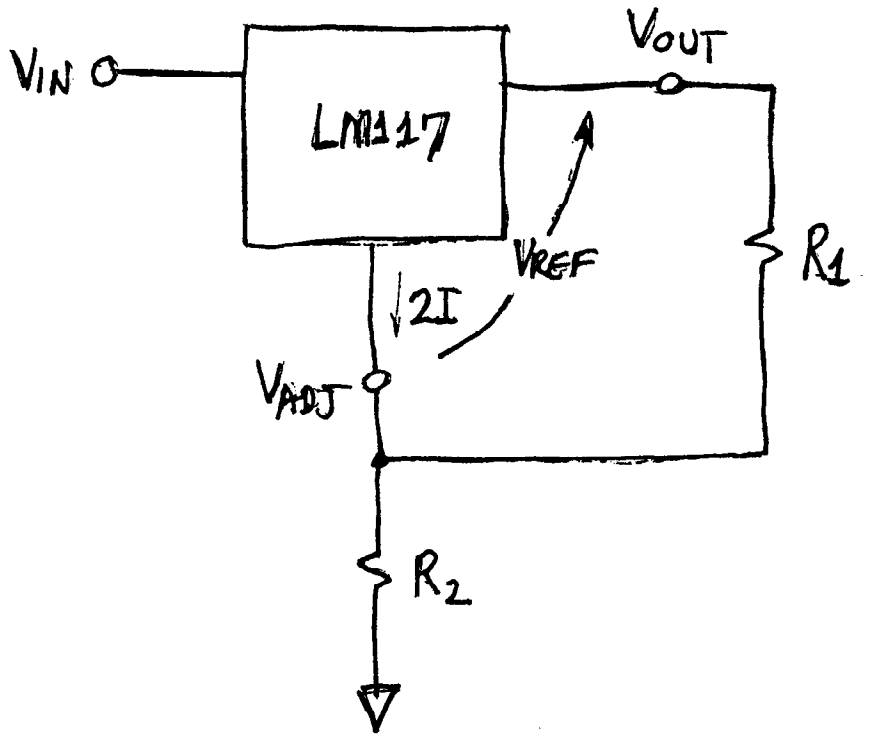
From equation (5) we can also compute I

$$I = \frac{1}{RE} \frac{kT}{q} \ln N \qquad (5)$$

or at room temperature

$$I = 25 \text{ uA} \qquad (15)$$

Application of this device is a shown in Figure 4. We can now compute V_{OUT} for a set of external adjustment resistors R_1 and R_2.



LM117 APPLICATION

FIGURE 4.

Note that

$$V_{OUT} = V_{REF} + \left(\frac{V_{REF}}{R_1} + 2I\right) R_2 \qquad (16)$$

or

$$V_{OUT} = V_{REF}\left(1 + \frac{R_2}{R_1}\right) + 2IR_2 \qquad (17)$$

$2IR_2$ is an error term and should be minimized by keeping R_2 as small as practical. Note that this implies that the current through R_1 (V_{REF}/R_1) completely swamps 2I. In typical application $R_1 = 240\ \Omega$, resulting in a 5mA current through R_1. Thus we may safely say that

$$V_{OUT} \cong V_{REF}\left(1 + \frac{R_2}{R_1}\right). \qquad (18)$$