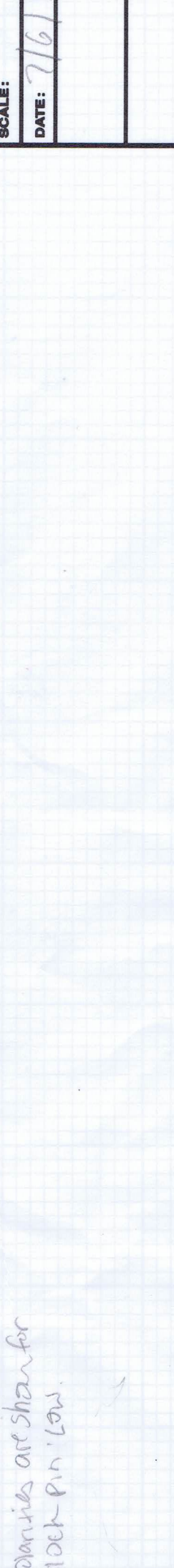
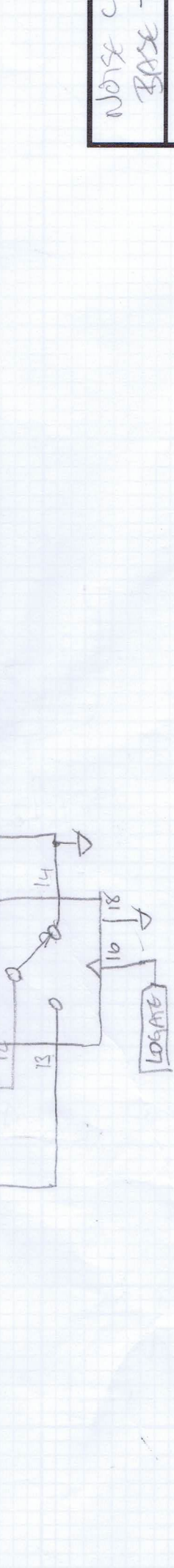
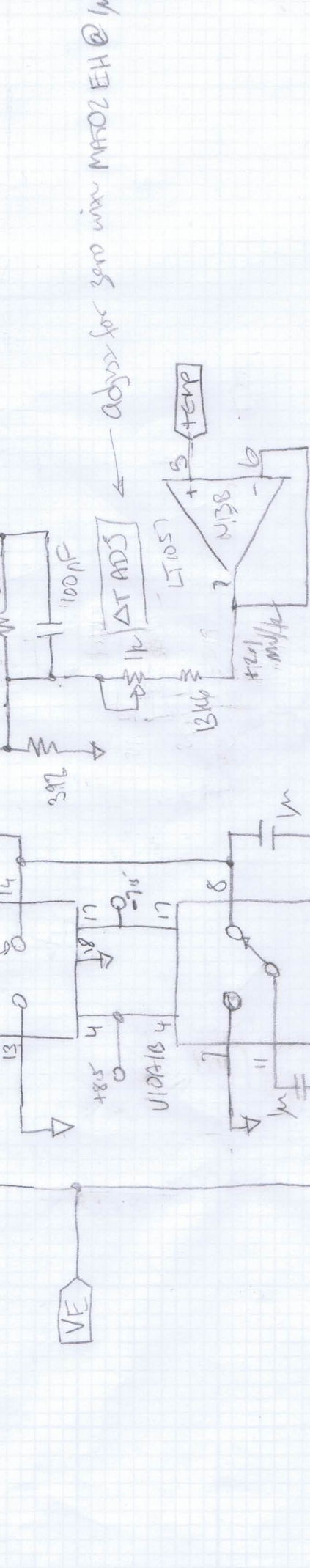
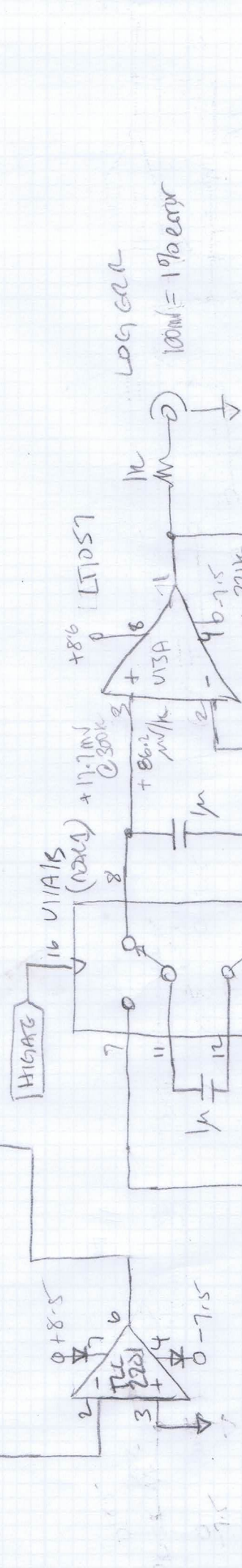
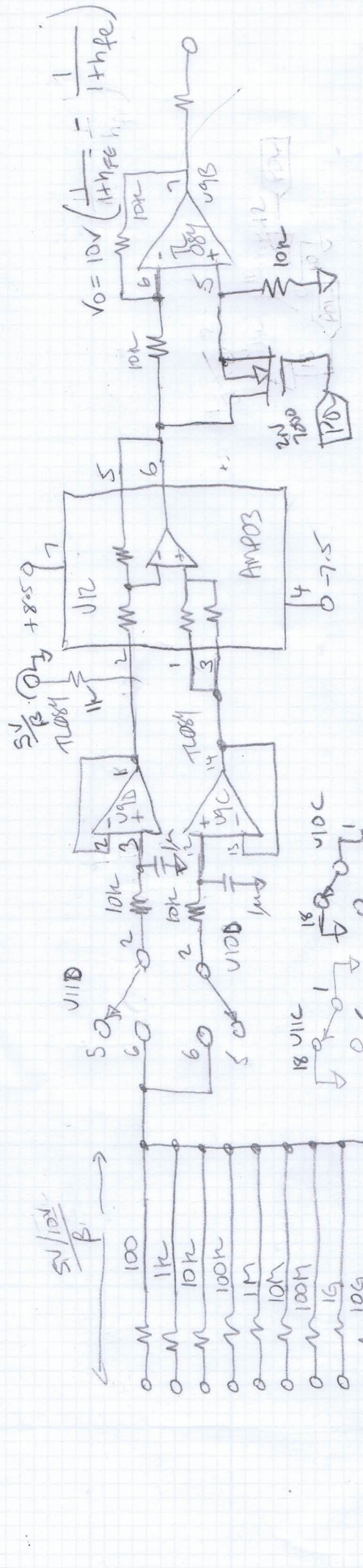


$h_{fe} > h_{fe} \rightarrow$  pos (PWR)  
neg (MFW)

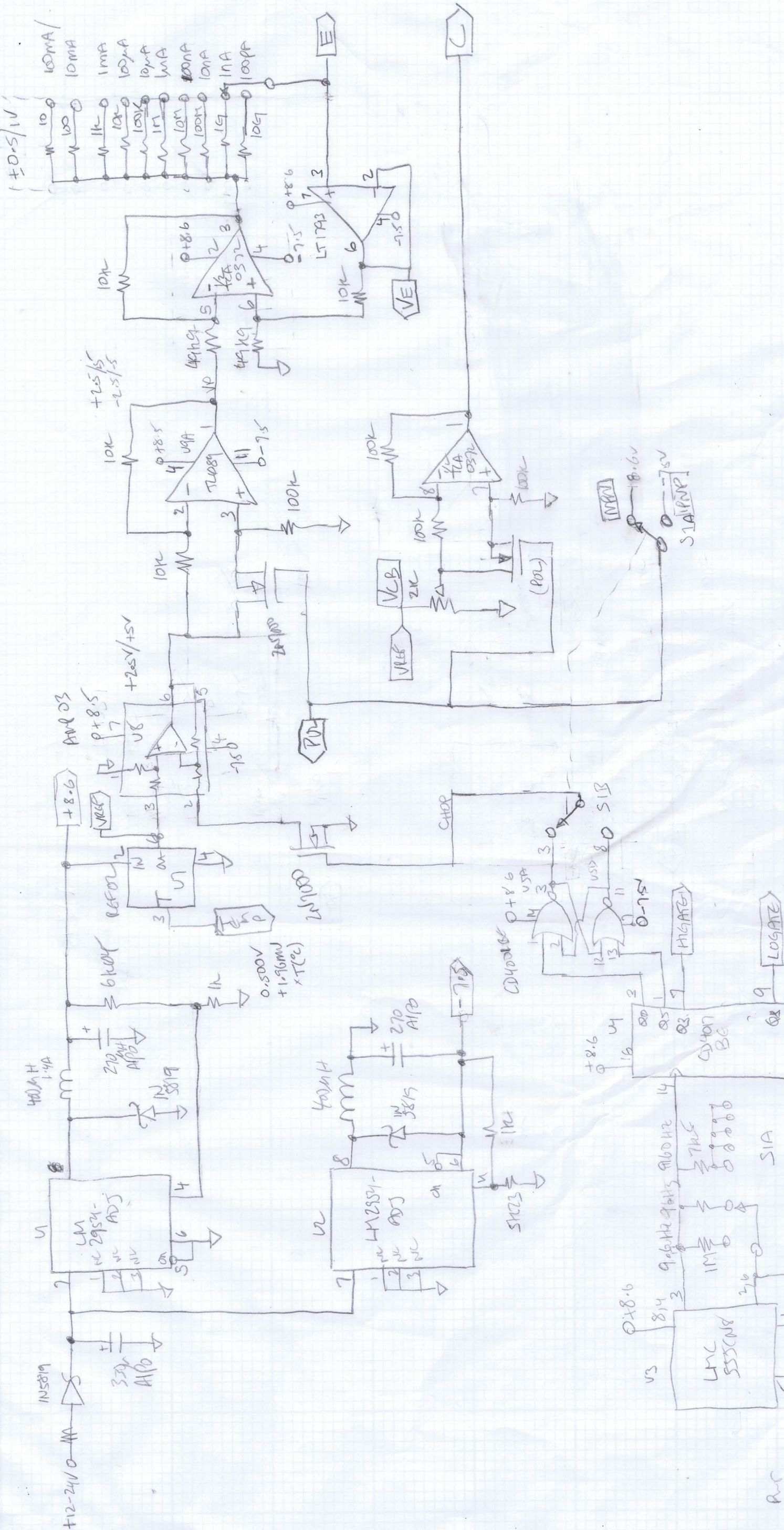


adjust for zero with MFOZ EH @ 1mA IDMA

NOISE CANCELLED TRANSISTOR TESTER  
BASE TIA & LOG CONFORMANCE SECTIONS

SCALE:	APPROVED BY:	DRAWN BY T-Hobbes
DATE: 7/6/13		REVISED
		DRAWING NUMBER

Notes  
1: Polarities are shown for clock pin 'Low'



NOISE CANCELER TRANSISTOR TESTER  
 SEQUENCING AND GATE-DRIVER

SCALE: \_\_\_\_\_ APPROVED BY: P.Hobbs

DATE: 7/6/13 REVISED

DRAWING NUMBER

REVISED 7/6/13